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NEC304

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131315

Roll No. | | | | | | | | | | |

B.Tech. (Semester-III)

SPL. THEORY EXAMINATION, 2014-15

SWITCHING THEORY LOGIC DESIGN

Time : 2 Hours] *[Total Marks : 50*

1. Attempt any two parts: 6×2=12

(a) An asynchronous sequential logic circuit is described by the following excitation and output function:

$$y = X_1X_2 + (X_1 + X_2)Y$$

$$Z = y$$

Draw the logic diagram of the circuit. Also derive the transition table and output map.

(b) (i) Explain a $4X1$ mux.

(ii) Implement the logic expression $Y = \Sigma m(0, 1, 2, 3, 6, 7)$ using mux.

(c) Minimize:

$$y = \Sigma m(0, 1, 2, 3, 5, 6, 7, 8, 14, 15) + d(4, 11, 13)$$

using tabular method.

2. Attempt any <u>four</u> parts: 4×4=16

(a) Draw and explain single-bit magnitude comparator.

(b) Draw and explain the SISO, SIPO register.

(c) Implement a full adder using decoder and two or gates.

(d) Write the canonical form of

$$Y = (A+B)(B+C)(A+C)$$

(e) Simplify the following Boolean function using K-map:

$$Y = \Sigma m(0, 1, 2, 3, 4, 6, 7, 9, 11, 13, 15) + d(8, 12)$$

3. Attempt all <u>three</u> parts: 4×3=12

(a) Convert the following:

(i) $(ABC.75)_{16} = (?)_{10}$

(ii) $(467.342)_8 = (?)_{10}$

(b) What is race around condition? How it can be avoided.

(c) Generate the hamming code for the word 11011.

4. Attempt any <u>two</u> parts: 4×2=10

(a) Design a universal shift register that performs HOLD, SHIFT RIGHT, SHIFT LEFT and LOAD.

(b) Write the steps for combinational circuit designing and design a circuit of three input which gives an high output whenever the sum of LSB and MSB bit is 1.

(c) Draw and explain 3-bit by 2-bit multiplier.

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