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EC – 302

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3003 Roll No. | | | | | | | | | | |

B.Tech.

THIRD SEMESTER EXAMINATION, 2004-2005

SWITCHING THEORY AND LOGIC DESIGN

Time : 2 Hours *Total Marks : 50*

Note : *Attempt ALL the questions.*

1. Answer ***any two*** parts of the following : **[5 x 2 = 10]**

(a) Minimize f = Π(1,4,5,6,11,12,13,14,15) using K – map.

(b) Minimize f = Σ (0,1,2,3,4,6,7,8,9,11,15) using Tabular method.

(c) Explain with example, how don't care conditions are implemented in K-map minimization.

2. Answer ***any two*** of the following : **[7 x 2 = 14]**

(a) Discuss with design n - to – 2^n decoder.

(b) Implement four variable switching function using multiplexer, f = Σ (0,2,4,6,8,10,12) for representing negative numbers.

(c) Explain 2's complement method for representing negative numbers using example.

3. Answer *any two* parts of the following : **[6 x 2 = 12]**

(a) Draw and explain working of Master – Slave JK Flip-flop.

(b) Implement modulo – 8 binary counter with SR flip-flops.

(c) Discuss the difference between synchronous circuits with example.

4. Answer *any two* of the following : **[7 x 2 = 14]**

(a) Discuss the concept of partial flow table and primitive flow table to design fundamental mode asynchronous sequential circuit.

(b) Explain the races and cycles with appropriate avoidance technique.

(c) Briefly explain n – bit error detecting code.

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