EC-302

B.TECH.

THIRD SEMESTER EXAMINATION, 2001-2002
SWITCHING THEORY & LOGIC DESIGN

Time—2 Hours   *Total Marks—50*

Note : Answer *ALL* the questions.

1. Attempt any *Two* parts. All parts carry equal marks.   4 × 2

    (*a*) Simplify the Boolean function F in Sum-of-product using the don't – care conditions d :

    $$F = B'C'D' + BCD' + ABCD'$$
    $$d = B'CD' + ABC'D$$

    (*b*) Simplify the following Boolean function by means of the tabulation method :—

    $$F(A, B, C, D) = \sum (4,6,7,8,9,10,11,15)$$

    (*c*) The following Boolean Expression :

    $BE + B'DE'$ is a simplified version of expression :—

    $$A'BE + BCDE + BC'D'E + A'B'DE' + B'C'DE'.$$

    Are there any don't-care conditions ? If so, what are they ?

2. Attempt any *Four* parts. All parts carry equal marks.   3½ × 4

    (*a*) (*i*) Find the decimal equivalent of the following binary numbers assuming signed magnitude representation of the binary number :—

        (1) 001000

        (2) 1111

(*ii*) Write the procedure for the subtraction of two numbers with $(r-1)$'s complement.

(*b*) Perform the subtraction with the following binary numbers using (1) 2's complement (2) 1's complement.

(*i*) 11010 – 1101

(*ii*) 10010 – 10011

(*c*) Perform the subtraction with following decimal numbers using (1) 10's complement (2) 9's complement.

(*i*) 5294 – 749

(*ii*) 27 – 289

(*d*) Implement the following function with a 4×1 multiplexer.

$$F(A, B, C) = \sum (1, 3, 5, 6)$$

(*e*) Implement a full-adder circuit with a 3×8 decoder and two *OR*-gates.

(*f*) What is Hazards ? How will you design a Hazard-free switching circuit ?

3. Attempt any *Four* parts. All parts carry equal marks. $3\frac{1}{2} \times 4$

(*a*) How will you differentiate between combinational circuit and sequential circuit.
Consider a J–K' flip-flop, i.e. a J–K flip-flop with an inverter between external input K' and internal input K.

(*i*) Obtain the flip-flop characteristic table.

(*ii*) Obtain the characteristic equation.

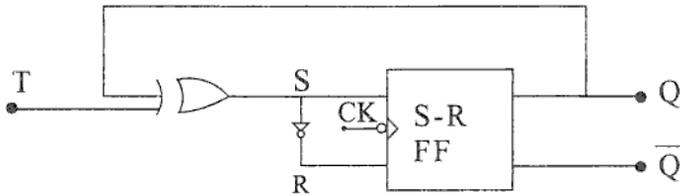(b) Prepare the truth-table for the circuit of fig-3b and show that it acts as a T-flip-flop.

Figure-3b

(c) A mod-3 counter (reset after every three pulses) is shown in fig-3c. The flip-flops used are master-slave J-K. Sketch the waveform of Q_0 and Q_1 when clock pulses are applied and verify its operation. Assume $Q_0 = Q_1 = 0$ initially.
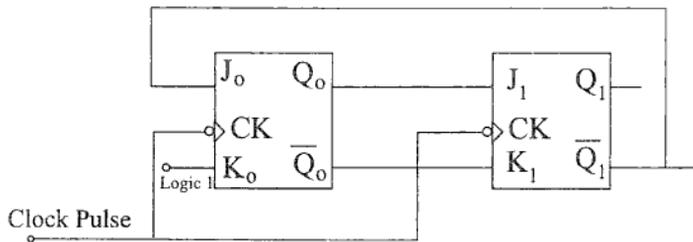

Figure-3c

(d) What is race-around condition ?

If $\overline{Q}$ output of a D-type flip-flop is connected to D-input, it acts as a toggle switch, verify.

(e) For the state diagram shown in figure-3e, obtain the state table and design the circuit using minimum number of J-K flip-flop.
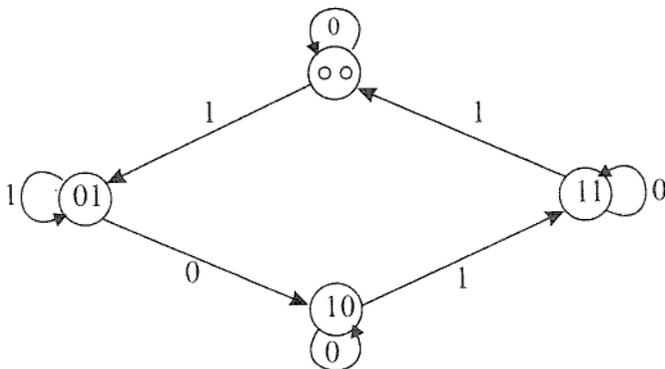

Figure-3e

(f) Design a 3-bit binary UP/DOWN counter with a direction control M. Use J-K flip-flop.

4. Attempt any *Four* parts. All parts carry equal marks. $3\frac{1}{2} \times 4$

(a) Explain the principle of constructing a Hamming error-correcting code. Construct a Seven-bit Hamming code for the 4-bit message 0100.

(b) Explain the floating-point data representation for decimal number and binary number. When is a floating point number said to be normalized ?

(c) What is the difference between asynchronous and synchronous circuits ? Represent the Octal number $(17.32)_8$ into floating point Octal number and floating point binary number.

(d) Draw the basic model for fundamental mode circuits and explain.