Roll No: | | | | | | | | | | | | | |

BTECH
(SEM III) THEORY EXAMINATION 2021-22
DIGITAL SYSTEM DESIGN

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief: 2 x 10 = 20

Qno.	Question	Marks	CO
a.	Simplify the expression F (A, B, C) = AB+BC+A' by K- Map.	2	1
b.	Discuss the concept of fan-in and fan-out?	2	3
c.	What is the role of subtractor in digital electronics?	2	3
d.	Construct half subtractor using NAND gates.	2	4
e.	Distinguish between shifter and barrel shifter?	2	3
f.	Define ASM and FSM?	2	4
g.	Why ECL is fastest logic family?	2	3
h.	What do you understand by digital TTL?	2	4
i.	List some advantages of successive approximation?	2	2
j.	Where is SAR ADC used?	2	5

SECTION B

2. Attempt any *three* of the following: 3 x 10 = 20

Qno.	Question	Marks	CO
a.	Write the differences between combinational and sequential circuits.	10	1
b.	Design 2-bit magnitude comparator.	10	2
c.	Explain the working of Master-Slave JK flip-flop with the help of logic diagram, functional table, logic symbol.	10	3
d.	i) Draw and explain block diagram of Moore model and Mealy model. ii) Write the difference between ripple counter and synchronous counter.	10	3
e.	List the guidelines for construction of state graphs.	10	4

SECTION C

3. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Minimize the following Boolean function- F(A, B, C, D) = Σm(0, 3, 4, 5, 7, 9, 13, 14, 15)	10	1
b.	Expand the following into canonical form and represent in decimal form: i) f1 = a+bc+ac'd into min terms. ii) f2 = a(b+c) (a+c+d) into max terms	10	1

4. Attempt any *one* part of the following: 1 x 10 = 10

a.	Explain the concept of serial adder with accumulators.	10	2
b.	Design a full adder by constructing the truth table and simplify the output equations.	10	2

5. Attempt any *one* part of the following: 1 x 10 = 10

a.	Design a mod 11 up ripple counter using T-FF.	10	3
b.	Explain positive edge triggered D-flip-flop with the help of circuit diagram and waveforms.	10	3

6. Attempt any *one* part of the following: 1 x 10 = 10

a.	Draw a circuit diagram of a CMOS inverter. Draw its transfer characteristics and explain its operation.	10	4
b.	With the help of a neat diagram, explain the working of a two-input TTL NAND gate.	10	4

7. Attempt any *one* part of the following: 1 x 10 = 10

a.	Explain single slope and dual slope ADC with a neat sketch.	10	5
b.	Describe switched capacitor and write its applications.	10	5