PAPER ID-311408

Roll No:

BTECH
(SEM III) THEORY EXAMINATION 2023-24
DIGITAL SYSTEM DESIGN

TIME: 3HRS   M.MARKS: 70

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1.	Attempt *all* questions in brief.	2 x 7 = 14	
Q no.	Question	Marks
a.	What is the purpose of binary arithmetic in digital logic design?	2
b.	Explain the concept of signed magnitude representation.	2
c.	Explain the operation of a multiplexer.	2
d.	How does a full adder differ from a half adder?	2
e.	What are the basic building blocks of sequential logic circuits?	2
f.	What is fan-out in logic families?	2
g.	What are the key specifications of a DAC?	2

SECTION B

2.	Attempt any *three* of the following:	7 x 3 = 21	
a.	Convert the following. Hexadecimal equivalent of the decimal number 256 Decimal equivalent of (123)9 378.9310 to octal Convert A3BH and 2F3H into binary.	7
b.	Design a full adder by constructing the truth table and simplify the output equations.	7
c.	Describe the operation of various flip-flops, including S-R, JK, D, and T flip-flops	7
d.	Draw a circuit diagram of a CMOS inverter. Draw its transfer characteristics and explain its operation.	7
e.	Explain switched capacitor and give its applications	7

SECTION C

3.	Attempt any *one* part of the following:	7 x 1 = 7	
a.	Use Karnaugh maps to simplify the Boolean function: F(A, B,C,D) = Σ(1, 2, 4, 6, 9, 10, 11, 12, 13, 14, 15).	7
b.	State and Prove Demorgan's theorem.	7

4.	Attempt any *one* part of the following:	7 x 1 = 7	
a.	Implement a full adder using NAND gates.	7
b.	Design 2-bit magnitude comparator.	7

5.	Attempt any *one* part of the following:	7 x 1 = 7	
a.	Compare and contrast Mealy and Moore machines and discuss their applications in digital systems design.	7
b.	Explain positive edge triggered D-flip-flop with the help of circuit diagram and waveforms.	7

6.	Attempt any *one* part of the following:	7 x 1 = 7	
a.	Explain the characteristics and specifications of TTL NAND gates, including noise margin, propagation delay, fan-in, and fan-out.	7
b.	Describe the concept of programmable logic devices (PLDs) and explain how they are used for logic implementation in digital systems.	7

7.	Attempt any *one* part of the following:	7 x 1 = 7	
a.	Explain the principle of operation of an R2R ladder DAC.	7
b.	Describe the principle of operation of a successive approximation ADC.	7

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