PAPER ID-411807

Roll No: | | | | | | | | | | | |

BTECH
(SEM III) THEORY EXAMINATION 2021-22
DIGITAL LOGIC DESIGN

Time: 3 Hours   *Total Marks: 70*

Note: **1.** Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1.   **Attempt *all* questions in brief.**   **2 x 7 = 14**

a.	Define Pair, Quad, and Octet.
b.	Describe sign magnitude representation.
c.	Compute (i) BCD, (ii) excess-3 code, (iii) 2421 code, and (iv) a 6311 code of a decimal number 4125.
d.	Explain difference between latch and flip-flop.
e.	Explain race around condition in brief.
f.	Implement the function $F = \bar{A}\bar{B}C + ABC\bar{D} + \bar{A}BCD + AB + C$ using PLA.
g.	Compute address lines and input-output data lines are needed in 64K x 8 memory units.

SECTION B

2.   **Attempt any *three* of the following:**   **7 x 3 = 21**

a.	Solve the following Boolean functions by using K-Map: $F(a, b, c, d) = \sum(0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$
b.	Explain the sequential logic circuits? Sketch the logic diagram of JK Flip Flop.
c.	Explain different logic gates families in digital circuits. Write a short note on Universal Gate.
d.	Write short notes on the following: i) Comparison between PROM, PLA and PAL. ii) Structure of 4-byte diode ROM.
e.	i) Design a 4-bit magnitude comparator using combinational gates. ii) Design a 4-bit priority encoder

SECTION C

3.   **Attempt any *one* part of the following:**   **7 x 1 = 7**

(a)	Solve the following logic function and realize using NOR gates. i) $F(a, b, c, d) = \prod(1, 2, 3, 7, 10, 11) + D(0, 15)$ ii) $F(a, b, c, d) = \prod(3, 4, 5, 6, 7, 10, 11, 15)$
(b)	Solve the following Boolean function using tabular method (Quine Mc-Clusky method): $F(A, B, C, D, E) = \sum(0, 2, 4, 10, 15, 19, 23, 29, 31)$

4.   **Attempt any *one* part of the following:**   **7 x 1 = 7**

(a)	Explain address multiplexing block diagram for a 64K DRAM.
(b)	Explain the hazards in combinational and sequential circuit. Also explain the remedy for eliminating a hazard.

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5.   **Attempt any *one* part of the following:**   **7 x 1 = 7**

| (a) | Design a Mod 6 synchronous counter using D flip-flop and T flip-flop. |
| (b) | With the help of logic diagram, explain the 4 bit universal shift register using D flip-flops and 4:1 MUX. |

6.   **Attempt any *one* part of the following:**   **7 x 1 = 7**

| (a) | Design a carry look ahead 4-bit parallel adder. Show that the time for addition is independent of the length of operands. |
| (b) | Construct 16:1 MUX using 4:1 and 2:1 multiplexers and hence analyze using truth table. |

7.   **Attempt any *one* part of the following:**   **7 x 1 = 7**

| (a) | Construct a state diagram for synchronous decade UP/DOWN counter. The mode control; 'M' decides the pattern of counting operation. When M=0 Counter counts UP and when M=1, counter counts DOWN. When counter reaches terminal count Y=1 (for UP count) and Z=1 (for DOWN count). Label the state diagram in M/YZ mode. |
| (b) | Explain the static RAM and dynamic RAM. Describe the PLA and its application in detail. |