PAPER ID-411797

Roll No: | | | | | | | | | | | | | |

BTECH
(SEM III) THEORY EXAMINATION 2021-22
DIGITAL LOGIC DESIGN

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 10 = 20

a.	Implement the following expression using NOR gates: F (w, x, y, z) = w′x′ + x′z′
b.	Compute 9's and 10's complement of the following decimal numbers: i) 24,681,234 ii) 63,325,600
c.	Construct 4 input priority encoder using combinational gates.
d.	Sketch the logic diagram of half subtractor.
e.	Explain error detecting and correcting codes.
f.	Define setup time.
g.	Illustrate Ring counter and Johnson counter.
h.	Sketch square wave output using D flip-flop.
i.	Explain shift registers.
j.	Explain primitive flow table.

SECTION B

2. Attempt any *three* of the following: 10x3=30

a.	Solve the logic function given below, using Quine McClusky minimization technique and realize simplified expression using universal gates. F(A, B, C, D) = ∑m(0, 1, 3, 7, 8, 9,11, 15)
b.	Design a 4-bit binary counter with parallel load.
c.	Explain the static RAM and dynamic RAM. Describe the PLA and its application in detail.
d.	Explain flow table and race conditions in asynchronous sequential circuit design.
e.	Show that the characteristic equation for the complement output of JK flip-flop is Q′(t+1) = J′Q′ + KQ

SECTION C

3. Attempt any *one* part of the following: 10x1=10

a.	Simplify the Boolean function F(A, B, C, D): ∑(1, 3, 7, 11, 12, 13) which has the don't care condition d(A, B, C, D): ∑(0, 2, 5, 9) and then express the simplified function in sum-of-minterms forrn.
b.	Explain different logic gates families in digital circuits. Write a short note on universal gate.

4. Attempt any *one* part of the following: 10x1=10

a.	Draw and explain the carry look ahead adder.
b.	What is asynchronous counter? How would you design asynchronous counter?

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5. Attempt any *one* part of the following: 10x1=10

a.	Explain the truth table of the SR, JK, D & T flip-flops.
b.	Design a Mod 6 synchronous counter using D flip-flop and T flip-flop.

6. Attempt any *one* part of the following: 10x1=10

a.	Explain PLA with the help of block diagram.
b.	Design a 4-bit binary up down ripple counter, also show its clock diagram.

7. Attempt any *one* part of the following: 10x1=10

a.	Describe the general procedures that must be followed to ensure a race-free state assignment with example.
b.	Explain flow table and race conditions in asynchronous sequential circuit design.