Sub Code:NEC309

Paper Id: 130318 Roll No:

B TECH
(SEM-III) THEORY EXAMINATION 2019-20
DIGITAL LOGIC DESIGN

Time: 3 Hours *Total Marks: 100*

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 10 = 20

a. What is a Logic gate?
b. What is meant by a bit, pair, and quad?
c. What are the advantages and disadvantages of the K-Map Method?
d. What are the differences between Combinational Circuits and Sequential Circuits?
e. What are the applications of the octal number system?
f. Define Hold time?
g. What is Full-Adder?
h. Implement the Boolean function F = x'yz' + z using NOR gates only.
i. Perform the BCD addition of 256 and 85.
j. Convert the Gray Code 111001 into binary code.

SECTION B

2. Attempt any *three* of the following: 10x3=30

a. Define Multiplexer. Give the example of 4×1 multiplexer. Draw its truth table.
b. Using active high output 3:8 line decoder, implement the following functions
f1(A,B,C,D)=Σ m(0,1,2,5,7,11,15)
f2(A,B,C,D)=Π m(1,3,4,11,13,14)
c. Design a carry look ahead 4-bit parallel adder. Show that the time for addition is independent of the length of operands
d. Using Quine McCluskey method & PI reduction table, determine the minimal SOP expression for the following using decimal notation
f=Σ m(1,4,7,9,12,14)+Σ d(2,13)
e. Draw a circuit diagram of a CMOS inverter. Draw its transfer Characteristics and explain its operation.

SECTION C

3. Attempt any *one* part of the following: 10x1=10

a. Design a synchronous counter using JK flip-flops to count the sequence 0,1,2,4,5,6,0,1,2 use static diagram and state table
b. Write the truth table of the SR, JK, D & T flip-flops.

4. Attempt any *one* part of the following: 10x1=10

a. Design a combinational circuit that accepts a three bit number and generates an output binary number equal to the square of the input number.
b. Design a BCD counter with JK flip flops.

5. Attempt any *one* part of the following: 10x1=10

a. Simplify following logic function and realize using NOR gates.
f(w,x,y,z)=πM(1,2,3,7,10,11)+d(0,15)
f(w,x,y,z) = π M (3,4,5,6,7,10,11,15)
b. Draw the basic circuit fo the DTL NAND gate. Explain the operation.

6. Attempt any *one* part of the following: 10x1=10

a. Design a BCD toexcess-3 code converter using ROM
b. Convert the decimal number 246.8 to base 3, base 5 and base 7.

7. Attempt any *one* part of the following: 10x1=10

a. Draw the basic flip flop circuit with NAND gates. Explain its operation.
b. What is state reduction? Explain with a suitable example.