

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0323

Roll No.

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B. Tech.

(SEM. III) THEORY EXAMINATION, 2012-13

DIGITAL ELECTRONICS*Time : 3 Hours]**[Total Marks : 100***SECTION – A**1. Attempt **all** parts :**10 × 2 = 20**

- (a) What is the largest binary number that can be expressed with (i) 14 bits and (ii) 10 bits ?
- (b) Convert $(247.36)_8 = (?)_{16}$.
- (c) If the number of states of a counter is 8, then find the number of flip-flops required for it.
- (d) Simplify the following Boolean expression.

$$F = (AB + \bar{A}B + \bar{A}\bar{B})$$
- (e) What do you mean by Edge-triggering & Level-triggering in flip-flops ?
- (f) A 3-bit synchronous counter uses flip-flops with propagation delay time 20 ns each. Determine the maximum possible time required for change of state.
- (g) What is the maximum number of product terms in a minimal sum of products form of a function of n Boolean variables ?
- (h) What problem could occur when the counter circuit is powered-up ? Give two possible general methods for overcoming the problem.
- (i) How many address lines and input-output data lines are needed in $2M \times 8$ memory unit ?
- (j) Define Primitive Flow Table ?
- (k) What is the difference between an internal state and a total state ?

SECTION – B

2. Attempt any **three** parts.

3 × 10 = 30

(a) Given :

$$F = A \cdot B \cdot \bar{C} \cdot D + A \cdot C + B \bar{C} \cdot \bar{D} + \bar{B} \cdot C + \bar{A} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D$$

(i) Show using a K-map that F can be simplified to

$$F_1 = A \cdot B + \bar{A} \cdot \bar{B} + A \cdot C + B \cdot \bar{C} \cdot \bar{D}$$

(ii) Show that there are a total of four possible expressions for F.

(iii) Show F_1 can be implemented using NAND gates and draw the circuit diagram.

(b) Using four half-adders :

(i) Design a two-bit binary magnitude comparator.

(ii) Realize expression F using 8-to-1 multiplexer.

$$F = f(x, y, z) = \sum (1, 2, 4, 5, 7)$$

(c) Explain the working of a Master – Slave JK flip-flop with functional table and timing diagram. Show how race around condition of master-slave SR flip-flop is over come.

(d) Draw the Block Diagram, Data path and ASMD chart for a binary multiplier.

(e) Obtain a primitive flow table for a circuit with two inputs, x_1 and x_2 , and two outputs, z_1 and z_2 that satisfy the following four conditions.

(i) When $x_1 x_2 = 00$, the output is $z_1 z_2 = 00$

(ii) When $x_1 = 1$, and x_2 changes from 0 to 1, the output is $z_1 z_2 = 01$

(iii) When $x_2 = 1$, and x_1 changes from 0 to 1, the output is $z_1 z_2 = 10$

(iv) Otherwise, the output does not change.

SECTION – C

Attempt **all** parts :

5 × 10 = 50

3. Attempt any **one** part :

(a) The state of 9 bit register is 111011010. What is its content if it represents

(i) Three decimal digits in BCD ?

(ii) Three decimal digits in the excess-3 code ?

(iii) Three decimal digits in the 8-4-2-1 code ?

(iv) A binary number ?

- (b) Simplify the Boolean function $F = A'B'C' + BC'D' + A'BCD' + AB'C'$ using four-variable k-map. Explain briefly Prime Implicants.

4. Attempt any **one** part :

- (a) (i) Design a BCD to Excess-3 Code Converter.
(ii) Explain different types of RAM & ROM.
- (b) Implement the following Boolean function with a PLA
(i) $F(A, B, C, D) = \sum (0, 2, 5, 7, 11, 14)$
(ii) $F(A, B, C) = \sum (0, 3, 5, 7)$

5. Attempt any **one** part :

- (a) Design a Mealy and Moore state machines for the detection of sequence 0101.
- (b) A sequential circuit has two JK flip-flops A and B and input x. The circuit is described by the following flip-flop input equations.

$$J_A = Bx + B'y' \quad K_A = B'xy'$$

$$J_B = A'x \quad K_B = A + xy'$$

- (i) Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the J and K variables.
- (ii) Draw the state diagram of the circuit.

6. Attempt any **one** part :

- (a) It is necessary to formulate the Hamming Code for four data bits D3, D5, D6 and D7, together with three parity bits P1, P2 and P4.
- (i) Evaluate the 7-bit composite code word for the data word 0010.
- (ii) Evaluate three check bits C4, C2 and C1 assuming no error.
- (iii) Assuming an error in bit D5 during writing into memory. Show how the error in the bit is detected and corrected.
- (b) (i) Derive the ROM programming table for the combinational circuit that squares a four-bit number.
- (ii) Minimize the number of product terms of part (i).

7. Attempt any **one** part :

- (a) Design a sequential 8-bit multiplier. You can assume that a 16-bit adder has been provided. The finite state control can be described by a state diagram.
 - (b) Explain Hazards in Combinational & Sequential Circuits.
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