Sub Code:EC302MTU

Paper Id: 130305 Roll No:

B.TECH
(SEM-III) THEORY EXAMINATION 2019-20
DIGITAL DESIGN

Time: 3 Hours *Total Marks: 100*

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 10 = 20

a. What is the best Example of Digital system?
b. Define Pair, Quad, and Octet?
c. What are the basic Logic gates?
d. Define Fan-in and Fan-out?
e. What are the fundamental properties of Boolean algebra?
f. Define Setup time?
g. What is meant by K-Map or Karnaugh Map?
h. What is a Multiplexer?
i. Convert the Binary Code 111001 into octal and hexadecimal code.
j. Perform the BCD addition of 126 and 105.

SECTION B

2. Attempt any *three* of the following: 10x3=30

a. Explain the full adder circuit using logic diagram and Truth Table.
b. Explain different logic gates families in digital circuits. Write a short note on Universal Gate.
c. Solve the following Boolean functions by using K-Map : F (w,x,y,z) = Σ(0,1,4,5,6,8,9,10,12,13,14)
d. What is asynchronous counter? How would you design asynchronous counter?
e. What are sequential logic circuits? Draw the logic diagram of JK Flip Flop.

SECTION C

3. Attempt any *one* part of the following: 10x1=10

a. With the help of logic diagram, explain the 4 bit universal shift register using D flip-flops and 4:1 MUX.
b. Write the truth table of the SR, JK, D & T flip-flops.

4. Attempt any *one* part of the following: 10x1=10

a. Design a Mod 6 synchronous counter using D flip-flop and T flip-flop.
b. Explain Mealy and Moore model of a clocked synchronous sequential network.

5. Attempt any *one* part of the following: 10x1=10

a. Construct a state diagram for synchronous decade UP/DOWN counter. The mode control; 'M' decides the pattern of counting operation. When M=0 Counter counts UP and when M=1, counter counts DOWN. When counter reaches terminal count Y=1 (for UP count) and Z=1 (for DOWN count). Label the state diagram in M/YZ mode.
b. Define state, present state, state diagram and state table.

6. Attempt any *one* part of the following: 10x1=10

a. Implement 4 bit magnitude comparator.
b. Simplify following logic function and realize using NOR gates. $f(w,x,y,z)=\pi M(1,2,3,7,10,11)+d(0,15)$ $f(w,x,y,z) = \pi M (3,4,5,6,7,10,11,15)$

7. Attempt any *one* part of the following: 10x1=10

a. Design a carry look ahead 4-bit parallel adder. Show that the time for addition is independent of the length of operands.
b. Construct 16:1 MUX using 4:1 and 2:1 multiplexers and hence analyze using truth table.