(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1010 Roll No. | | | | | | | | | | |

B.Tech.

SEVENTH SEMESTER EXAMINATION, 2006-07

COMPUTER ARCHITECTURE

Time : 3 Hours *Total Marks : 100*

Note : *(i) Attempt ALL questions.*

(ii) All questions carry equal marks.

(iii) Be precise in your answer.

1. Attempt ***any four*** parts of the following : **(5x4=20)**

(a) Discuss various classifications of parallel processing mechanisms in uniprocessor computers.

(b) Comment on balancing of system bandwidth.

(c) Differentiate between parallel and distributed processing.

(d) Why array computers are termed as parallel computers ?

(e) Discuss static and dynamic dataflow architecture models in short.

(f) Elaborate Flynn's classification.

2. Attempt *any four* parts of the following : **(5x4=20)**

(a) Explain hierarchical memory system. What do you mean by hit ratio and failure ratio ?

(b) What is m-way interleaving ? Discuss different types of memory interleaving.

(c) Differentiate between super scalar and vector processors.

(d) Differentiate between DMA and I/O channel.

(e) How memory contention problem can be reduced in multiprocessor systems ?

(f) How multi cache coherence problem is handled ?

3. Attempt *any two* parts of the following : **(10x2=20)**

(a) What are pipeline hazards ? Elaborate on various types of hazards and indicate how each is controlled.

(b) Prove that K-stage linear pipeline can be at most K-times faster than that of non-pipelined serial processor.

(c) Discuss various advanced pipelined techniques.

4. Attempt *any two* parts of the following : **(10x2=20)**

(a) Write down parallel algorithms for SIMD matrix multiplication. Compare time complexities of SISD and SIMD matrix multiplication algorithms.

(b) In context of language features to exploit parallelism by way of concurrency, define the following terms :

- JOIN
- FORK
- Cobegin-end
- Fair scheduling
- Crect

(c) Discuss the functional architecture of SIMD multiprocessor systems.

5. Attempt *any two* parts of the following : **(10x2=20)**

(a) Explain various types of interconnect networks used in multiprocessor systems.

(b) Differentiate multiport memory and multistage network.

(c) What is the memory arbiter ? Discuss arbitration policies. Give the circuit diagram of the simple arbiter.

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