

BTECH
(SEM V) THEORY EXAMINATION 2018-19
COMPUTER ARCHITECTURE

Time: 3 Hours**Total Marks: 100****Note: 1.** Attempt all Sections. If require any missing data; then choose suitably.**SECTION A****1. Attempt all questions in brief. 2 x 10 = 20**

- a. What do you understand by Locality of Reference?
- b. What is the need of Bus Arbitration?
- c. What do you understand by displacement addressing?
- d. What is the difference between RAM and DRAM?
- e. Write short notes on Arithmetic Micro Operations.
- f. Give some examples of software interrupts.
- g. List three types of control signals.
- h. Give the examples of RISC and CISC instruction set architectures?
- i. What are the different types of mapping techniques used in Cache memory?
- j. What are the conditions for divide overflow?

SECTION B**2. Attempt any three of the following: 10 x 3 = 30**

- a. Write a program to evaluate the expression :

$$X = \frac{A - B + C * (D - E)}{C + G * H}$$

- i) Write a program by two-addressing format to evaluate.
- ii) Using an accumulator type computer with one address instructions.
- b. Perform the division process of 10100011 by 1011 (use a dividend of 8 bits).
- c. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
 - (i) How many bits are there in the operation code, the register code part and the address part?
 - (ii) Draw the instruction word format and indicate the number of bits in each part.
 - (iii) How many bits are there in the data and address inputs of the memory?
- d. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.
 - i. Formulate all pertinent information required to construct the cache memory.
 - ii. What is the size of cache memory?

SECTION C

3. Attempt any *one* part of the following: 10 x 1 = 10

- (a) Design 4-bit carry look ahead adder.
- (b) Explain the difference between vectored and non-vectored interrupt. Explain stating examples of each.

4. Attempt any *one* part of the following: 10 x 1 = 10

- (a) Draw the flow chart of Booth's Algorithm for multiplication and show the multiplication process using Booth's Algorithm for (+15) X (-13).
- (b) Write a program to evaluate the arithmetic statement.

$$P = \frac{(X - Y = Z) * (M * n - o)}{Q + R * S}$$

By using

- (i) Two address instructions
- (ii) One address instructions
- (iii) Zero address instructions

5. Attempt any *one* part of the following: 10 x 1 = 10

- (a) A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and 4 interface units, each with 4 registers. A memory mapped configuration is used. The two highest order bits of the address bus are assigned 00 for RAM, 01 for of the ROM and 10 for interface registers.
 - (i) How many RAM and ROM chips are needed?
 - (ii) Draw a memory address map for the system.
 - (iii) Give the address range in hexadecimal for RAM, ROM and interface.
- (b) Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.

6. Attempt any *one* part of the following: 10 x 1 = 10

- (a) Define interrupts. When a device interrupt occurs how the processor does determine which device has issued the interrupt?
- (b) Explain all the phases of instruction cycle.

7. Attempt any *one* part of the following: 10 x 1 = 10

- (a) Explain the basic concept of Hardwired and Software control unit with neat diagrams.
- (b) Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional?