Printed Pages – 4 CS – 702

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1010 Roll No. | | | | | | | | | | |

B.Tech.

FIFTH SEMESTER EXAMINATION, 2004-2005

COMPUTER ARCHITECTURE

Time : 3 Hours *Total Marks : 100*

Note : *Attempt **ALL** questions.*

1. Answer ***any four*** of the following : – **(5x4=20)**

(a) Make a comparative view of the salient features of conventional, sequential processing and parallel processing ?

(b) Describe in brief any two classifications of parallel architecture excluding given in Question 1 (e).

(c) Discuss Amdahl' law with illustration by graph.

(d) Describe any three metrics for the performance measure of parallel computing.

(e) Describe the Shore's method of classification of parallel architecture.

(f) Point out logically the need of parallel computing.

Answer *any four* of the following : – **(5x4=20)**

(a) Discuss the Direct and Associative cache mapping with diagram.

(b) What is memory interleaving ? Describe eight way lower order memory interleaving.

(c) Consider a cache M_1 and memory M_2 hierarchy with the following characteristics.

M_1 : 16K words, 50ns access time

M_2 : 1M words, 400ns access time

Assume eight-word cache blocks and a set size of 256 words with set associative mapping.

(i) Show the mapping between M_2 and M_1.

(ii) Calculate the effective memory access-time with a Cache hit ratio of $h = 0.95$.

(d) Discuss the architectural features of any two super scalar processors.

(e) Make a hierarchical view of the different memory types in increasing order of capacity. Comment on the access time.

(f) Explain the terms Inclusion Coherence and Locality with reference to memory hierarchy.

Answer *any two* of the following : – **(10x2=20)**

(a) Derive Speed up, Efficiency and Through put for a k stages and n tasks in a linear pipeline. Show the variation of performance cost ratio with different stages.

(b) For the five stage pipelined processor specified by the following reservation task.

(i) List the set of forbidden latency and collision vector.

(ii) What is the Minimum Average Latency MAL ?

	t_1	t_2	t_3	t_4	t_5	t_6
S_1	X					X
S_2		X			X	
S_3			X			
S_4				X		
S_5		X				X

(c) (i) Discuss the following terms :

Collision vectors, state diagram, single cycles, greedy cycles and MAL.

(ii) Explain Interlocks and Hazards.

4. Answer ***any two*** of the following : – **(10x2=20)**

(a) Describe in short the various language features for parallelism.

(b) Describe the parallel algorithm for the multiplication in 2D mesh.

(c) Describe a parallel addition algorithm on a S/MD architecture.

5. Answer ***any two*** of the following : – **(10x2=20)**

(a) Describe any five commonly used static interconnection network with the required number of links.

(b) (i) Discuss the perfect shuffle and its inverse mapping over sixteen objects.

(ii) Describe the generalised structure of a multistage interconnection network.

(c) Discuss the structure of a cross bar switched network with its applicability in a multi processor.

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