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Printed Pages : 4 **TCS – 401**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1067 Roll No.

B. Tech.

(SEM. IV) EXAMINATION, 2006-07

COMPUTER ORGANIZATION

Time : 3 Hours] *[Total Marks : **100***

Note : *Attempt **all** questions. All questions carry **equal** marks.*

1 Attempt any **two** parts of the following : **10×2=20**

(a) Discuss the required hardware, hardware algorithm for Booth Multiplication. Iterate your algorithm for the product **(+13)*(–15).**

(b) Design an arithmetic circuit with one selection variable **S** and two **n**-bit data inputs **A** and **B**. The circuit generates the following four arithmetic operations in conjunction with the input carry $\mathbf{C_{in}}$. Draw the logic diagram for the first two stages :

S	$C_{in} = 0$	$C_{in} = 1$
0	D = A + B	D = A + 1
1	D = A – 1	$D = A + \bar{B} + 1$

(c) Write a procedure to add two IEEE single-precision floating point numbers. Each number is represented by a **32**-element Boolean array.

2 Attempt any **two** parts of the following : **10×2=20**

(a) Draw the flowchart for the execution of a complete instruction in a basic computer.

(b) Discuss the design and logic of a microprogram sequencer.

(c) A computer has **16** registers, an ALU with **32** operations, and a shifter with eight operations, all connected to a common bus system.

(i) Formulate a Control Word for a micro-operation.

(ii) Specify the number of bits in each field of the control word and give a general encoding scheme.

(iii) Show the bits of the control word that specify the micro-operation **R4 ← R5 + R6.**

3 Attempt any **two** parts of the following : **10×2=20**

(a) Write the program to evaluate the expression

$$X=\frac{A^{*}\left[B+C^{*}(D+E)\right]}{F^{*}(G+H)}$$ using the Zero-Address instruction and One-Address instruction.

(b) Explain various addressing modes with suitable examples.

(c) What are the basic differences between a branch instruction, a call subroutine instruction, and program interrupt ?

4 Attempt any **two** parts of the following : **10×2=20**

(a) Information is inserted into a FIFO buffer at a rate of m bytes per second. The information is deleated at the rate of n bytes per second. The maximum capacity of the buffer is k bytes.

(i) How long does it take for an empty buffer to fill up when **m > n**?

(ii) How long does it take for a full buffer to empty when **m < n**?

(iii) Is the FIFO buffer needed if **m=n**?

(b) A DMA controller transfers **16-**bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at the rate of **2400** characters per second. The CPU is fetching and executing instructions at an average rate of **1** million instructions per second. By how much will the CPU be slowed down because of DMA transfer?

(c) Draw a flow chart that describes the **CPU-I/O** channel communication in the **IBM 370.**

5 Attempt any **two** parts of the following : **10×2=20**

(a) Drive the logic of one cell and of an entire word for an associative memory that has an output indicator when the unmasked argument is greater than (but not equal to) the word in the associative memory.

(b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of **2048** words from the main memory. The main memory size is **128 K*32.**

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of the cache memory ?

(c) A virtual memory has page size of **1K** words. There are eight pages and four blocks. The associative memory page table contains the following entries :

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU.
