Number of Printed Pages—5 **CS-401**

**B. TECH.**

FOURTH SEMESTER EXAMINATION, 2001-2002

**COMPUTER ORGANISATION**

*Time : Three Hours* *Total Marks : 100*

**Note** : 1. Attempt ALL questions.
2. All questions carry equal marks.

**1.** Answer any FOUR of the following :— (5×4)

*(a)* Convert the following :

(*i*) $(43{\cdot}125)_{10} \rightarrow (\ )_2$

(*ii*) $(6B{\cdot}28)_4 \rightarrow (\ )_2$

(*iii*) $(76A)_{16} \rightarrow (\ )_8$

(*iv*) $(11001010)_2 \rightarrow (\ )_{Gray}$

*(b)* Perform the following arithmetic operations in 8-bit registers. Use signed 2's complement notation. Indicate overflow/underflow, if any :—

(*i*) − 28 − (− 100)

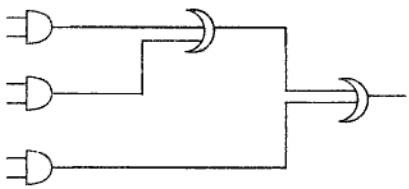
(*ii*) − 28 − 100

(*iii*) 78 − (− 49)

(*iv*) + 50 − 5

*(c)* Describe process of error-detection and correction. Give an example of error-detection code. Explain how it detects error.

(d) Transform the following logic ckts (without expressing its switching function) into an equivalent logic circuit that employs only 6NAND gates each with 2 inputs.



(e) Prove by Boolean Algebra :

(1) $A+(BC) = (A+B)\,(A+C)$

(2) $(A+B)(\overline{A}+C)(B+C)=(A+B)(\overline{A}+C)$

(f) Simplify the following Boolean function in product-of-sums form by means of a Four Variable map. Draw logic diagram with NOR gates.

$$F(w, x, y, z) = \Sigma\,(2,3,4,5,6,7,11,14,15)$$

**2.** Attempt any FOUR of the following :— (5×4)

(a) What is an ALU (Arithmetic Logic Unit) ? Draw logic diagram of ALU that performs AND, OR logic operations and ADD, SUB arithmetic operations.

(b) What is the purpose of counters ? How is ripple counter different to that of synchronous counter ? Draw logic diagram of 3 bit synchronous counter.

(c) Design a single 4 bit shift register which can be loaded parallel and serial, and read in parallel using R-S flip flop.

(d) What is the need of having many addressing modes in your machine ? Discuss Indirect and Displacement addressing in detail.

(e) What is a microoperation ? How can microoperation be used for execution of an instruction ? Explain with the help of an example.

(f) What is the meaning of the term one-address instruction ? How can an instruction which requires three operands be in such machine ? Explain with the help of an example.

**3.** Attempt any FOUR of the following :— (5 x 4)

(a) Give classification of Memory based on the method of access. Also discuss construction and working of Magnetic disk and various components of disk access time.

(b) What is the purpose of DMA module ? How can a DMA module be used for doing Input/Output from devices like Hand disks ? How is DMA different from that of Input/Output processor ?

(c) What is meant by the term 'BUS arbitration' ? Why is it needed ? How can bus arbitration be implemented is Daisy Chaining Scheme ?

(d) Describe any two mapping procedures for organisation of cache memory with example.

(e) Discuss various Semiconductor Memory cells. Also discuss a RAM organisation.

16 Kx 8 memory chips are used to construct 64 Kx16 memory :

(1) Find how many chips will be needed ?

(2) Draw block diagram showing connection of chips to address lines.

*(f)* What are the reasons for having interrupts in computers ? How can the interrupt be handled in the computers ? Suggest a scheme that can handle multiple interrupts at a time.

**4.** Attempt any FOUR of the following :— (5 x 4)

*(a)* Classify computers on the basis of Flynn's architectural scheme.

*(b)* Explain differences between parallelism and pipelining by implementation point of view.

*(c)* What are the various Branch handling mechanisms in pipelined processor ? Explain Delayed Branch and Branch Prediction mechanism.

**2.**

*(d)* Write an Assembly language program to replace a capital letter by lower case letter. Make suitable assumption, if any.

*(e)* Describe Strobe control, Handshaking for Asynchronous data transfer. What are advantages and disadvantages of both the methods ?

*(f)* What do you mean by procedure call & return in the assembly language ? How is it different from interrupt service routine ?

**5.** Write short notes on any FOUR of the following :— (5 x 4) 401

*(a)* Static RAM and Dynamic RAM

*(b)* Write through and Write block cache

*(c)* Memory mapped Input/Output and I/O mapped input/output

*(d)* Programmed Input/Output and Interrupt driven Input/Output 100

*(e)* RISC and CISC computers

*(f)* Hardwired and microprogrammed implementation

×4)