Roll No: | | | | | | | | | | | | | |

BTECH
(SEM III) THEORY EXAMINATION 2021-22
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours ***Total Marks: 70***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 7 = 14

a.	Describe the term addressing mode.
b.	Compare microinstruction and microprogram.
c.	Write decimal numbers 35 and -35 in 2's sign magnitude format.
d.	Define the term Memory Hierarchy in computer system.
e.	List the components of a typical I/O device interface.
f.	Explain speed up performance metric for a pipelined processor.
g.	Write one example of a 1-Address and 2-Address instruction.

SECTION B

2. Attempt any *three* of the following: 7 x 3 = 21

a.	Illustrate the designing of 3-bit carry look ahead adder.
b.	Differentiate between horizontal and vertical microinstruction. A vertical microprogrammed control unit supports 512 instructions. The system is using 8 conditional flags and contains 31 control signals. Each instruction on an average required 1 μ operation. Calculate the approximate size of control memory in bytes.
c.	Discuss the need of virtual memory. Demonstrate its implementation using paging.
d.	Describe serial communication technique in detail. Explain and compare the synchronous and asynchronous communication.
e.	Describe Flynn's classification in detail.

SECTION C

3. Attempt any *one* part of the following: 7 x 1 = 7

(a)	Illustrate the process of non-restoring division taking the division of $(13)_{10}$ by $(3)_{10}$.
(b)	Demonstrate floating-point number representation in computer, also give IEEE 754 standard 32-bit floating point number format of $(12.21)_{10}$ justifying each step.

4. Attempt any *one* part of the following: 7 x 1 = 7

(a)	Describe the working of microprogram sequencer with a suitable diagram and tables.
(b)	Explain hardwired control unit design using its block diagram. Explain generation of a control signal PC_{in} .

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5. Attempt any *one* part of the following: 7 x 1 = 7

(a)	Explain the interrupt driven I/O technique and design its flowchart in detail along with its merits and demerits.
(b)	Discuss the interrupt processing. Differentiate between the following: (i) Trap vs exception. (ii) Maskable and non-maskable interrupt.

6. Attempt any *one* part of the following: 7 x 1 = 7

(a)	A computer has a 256 K Byte, 4-way set associative, write back data cache with the block size of 32 Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition, to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. Solve for the number of bits in the tag field of an address. Explain each step of the calculation.
(b)	Calculate the number of page faults using optimal page replacement algorithm for the reference string: 1,5,4,3,2,5,1,2,4,3,6,4 if the number of frames in the memory is 3 and 4 illustrating each step.

7. Attempt any *one* part of the following: 7 x 1 = 7

(a)	(i) Justify the concept of Pipelining using a suitable diagram in a computer system. (ii) There is an instruction pipeline with four stages. The stage delays for each stage is 5 nsec, 6 nsec, 11 nsec, and 8 nsec respectively. Consider the delay of an inter-stage register in the pipeline is 1 nsec. Determine the approximate speedup of the pipeline in the steady state under ideal conditions as compared to the corresponding non-pipelined implementation?
(b)	Explain Cache performance measures. Evaluate the performance of 2-level Cache memory.