Sub Code: RCS302

Paper Id: 110302 Roll No: | | | | | | | | | | | | | |

B. TECH.
(SEM III) THEORY EXAMINATION 2019-20
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours *Total Marks: 70*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 7 = 14

a. Define Speedup Performance Laws.
b. Differentiate Linear and Nonlinear Pipeline Processors.
c. Differentiate interrupts and exceptions.
d. Show the bit configuration of 16 bit register when its contents represent the decimal equivalent of 250 in BCD.
e. Define the role of MIMD in computer architecture.
f. Define horizontal and vertical microprogramming.
g. What do you understand by locality of reference?

SECTION B

2. Attempt any *three* of the following: 7 x 3 = 21

a. Explain IEEE standard for floating point representation with example.
b. What is associative memory? Explain with the help of a block diagram. In addition, mention the situation in which associative memory can be effective utilized.
c. What do you mean by processor organization? Explain various types of processor organization.
d. What do you mean by high-speed adder? Discuss design of higher speed adders using block diagram.
e. Explain the different between vectored and non-vectored interrupt. Explain using example of each.

SECTION C

3. Attempt any *one* part of the following: 7 x 1 = 7

(a) Represent $(-456.1234)_{10}$ in single precision and double precision format.
(b) Explain the bus architecture with its types. Also, discuss the I/O bus architecture with block diagram.

4. Attempt any *one* part of the following: 7 x 1 = 7

(a) Register A holds the 8-bit binary 1111111. Determine the B operand and the logic micro operation to be performed in order to change the value in A to
  i. 01101111
  ii. 11111100
(b) Differentiate between Synchronous & asynchronous communication taking a suitable example.

5. Attempt any *one* part of the following: 7 x 1 = 7

(a) Write a program to evaluate the arithmetic statement

$$X = \big(A - B + C \times (D \times E - F)\big)/(G + H \times K)$$

  i. Using a general register computer with three address instructions.
  ii. Using an accumulator type computer with one address instruction.

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(b) Discuss Cache memories. What are the design issues? How performance is improved using the cache memories?

6. Attempt any *one* part of the following: 7 x 1 = 7

(a) A bit computer has 16-bit address bus. The first 15 lines of the address are used to select a bank of 32KB of memory. The higher order bit of the address is used to select a register, which receives the contents of the data bus. Explain How this configuration can be used to extend the memory capacity of the system to eight banks of 32KB each, for a total of 256 bytes of memory.

(b) List and explain the Modes of Data Transfer using block diagram.

7. Attempt any *one* part of the following: 7 x 1 = 7

(a) Show the systematic multiplication process $(20) \times (-19)$ using Booth's Algorithm.

(b) Explain and classify the Architectural Classification Schemes and differentiate between them.