Printed Pages: 02 **Sub Code: EEC201**

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B. TECH.
(SEM II) THEORY EXAMINATION 2018-19
ELECTRONICS ENGINEERING

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2×10 = 20**

a. How depletion layer is formed in a PN junction?
b. Calculate PIV of half wave and full wave rectifier.
c. Calculate the collector and emitter current levels of a BJT with α=0.99 and I_B=20μA.
d. Why CE configuration is widely used in Amplifier circuits?
e. Determine the value of gm for a JFET when IDSS=8mA, VP= ─ 6V and biased at VGS=VP/4.
f. Enlist the practical characteristics of OPAMP.
g. Convert 101 into equivalent binary and octal.
h. Why delay line is used in CRO?
i. Compare analog and digital instruments.

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a. (i) Draw and explain the working of Bridge rectifier with input and output waveforms.
(ii) Draw the output waveform for the circuit shown in fig (1).

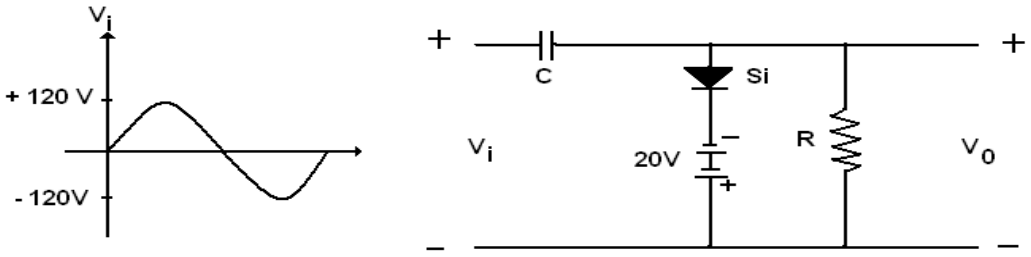

Fig (1)

b. (i) Draw the common emitter (CE) circuit of a transistor. Sketch its input and output characteristics curve. Indicate its various region of operation.
(ii) A junction transistor has the following h-parameter hie = 2kΩ, hre = $1.6x10^{-4}$, hfe = 50, hoe = 50μA/V. Determine Current Gain, Voltage Gain, Input Resistance, Output Resistance of the CE amplifier, if load resistance is 12 KΩ.

c. (i) Draw and explain construction and working of n- channel JFET and also plot the drain and transfer characteristics curves.
(ii). Calculate the output voltage V0 for the circuit of fig (2). Given that R_1 = 11 KΩ, R_2 = 22 KΩ, R_3 = 33 KΩ, R_f = 132 KΩ, and Vin = 20μV.

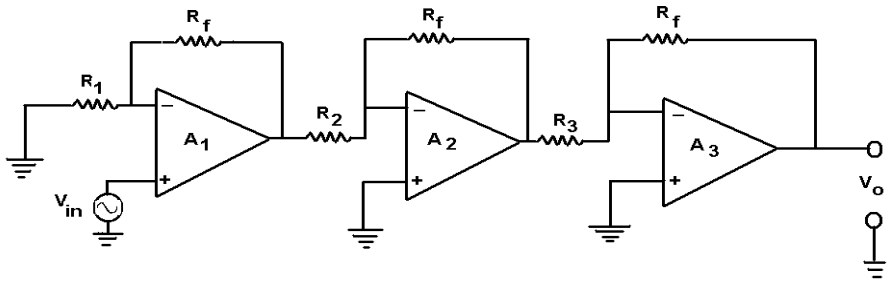

Fig (2)

d. (i) Convert the following numbers as indicated $(360)_8 = (\ldots\ldots..)_{16}$, $(10011.1101)_2 = (\ldots\ldots\ldots)_8$ and $(222.62)_{10} = (\ldots\ldots\ldots..)_{16}$.

(iii) Simplify the logic expression using Boolean algebra

$$f(A,B,C,D) = A\,\bar{B}\,\bar{C}D + \bar{A}\,\bar{B}\,D + BC\,\bar{D} + \bar{A}\,B + B\bar{C}$$

e. (i) Draw the block diagram of Digital Volt Meter (DVM). Also explain the function of each block.

(ii) Explain, how the signal pattern displayed over the CRO screen?

SECTION C

3. Attempt any *one* part of the following: 10 x 1 = 10

(a) Distinguish between Avalanche and Zener breakdown mechanism. Calculate I_R, I_Z, I_L and V_L for the network shown in fig (3) if R_L=470 Ω.

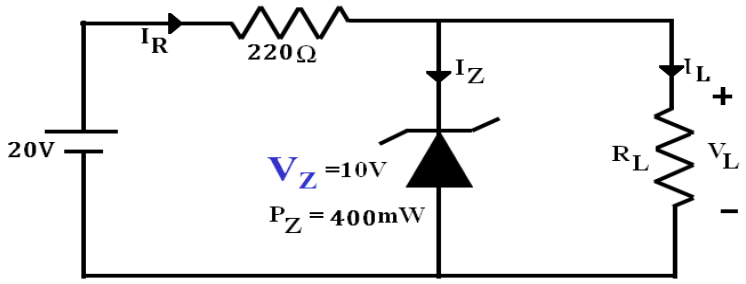

Fig (3)

(b) What is multiplier circuit? Draw the output waveform V_0 for the fig (4).

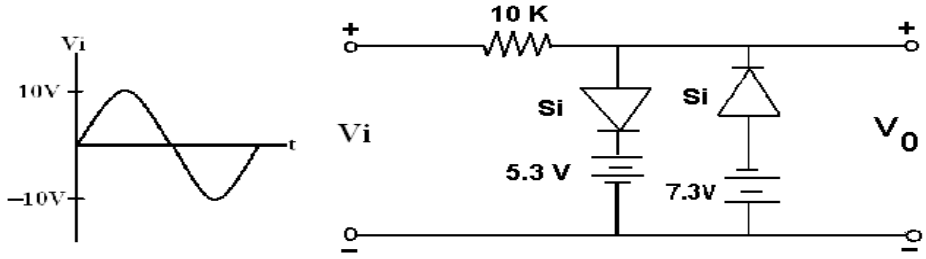

Fig (4)

4. Attempt any *one* part of the following: 10 x 1 = 10

(a) Draw the circuit for potential divider biasing with following parameters R_1=8.1KΩ, R_2=2.2KΩ, R_C=2.7KΩ, R_E=1.8KΩ, β=120, V_{CC}=20V. Also determine I_B, I_C, V_{CE}, V_E, V_C, V_B, and V_{BC}.

(b) Compare CE, CB and CC configuration of a BJT.

5. Attempt any *one* part of the following: 10 x 1 = 10

(a) Sketch the structure of an n-channel depletion mode MOSFET. Explain the drain and transfer characteristics. And also explain how depletion type MOSFET works as enhancement type MOSFET.

(b) Write short notes on Non inverting and Subtractor OPAMP. Find V_0 for the network shown in fig (5).

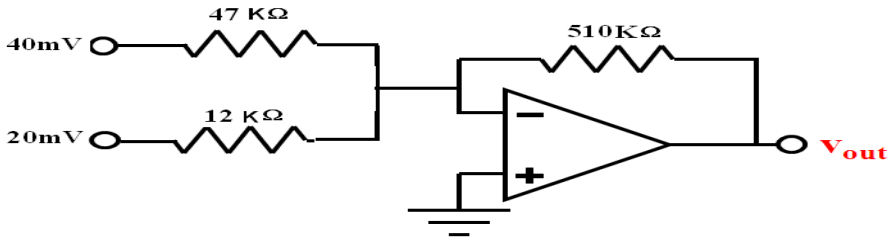

Fig (5)

6. Attempt any *one* part of the following: 10 x 1 = 10

(a) Reduce the function $f(A,B,C,D) = \Sigma m(1,3,7,11,15) + \Sigma d(0,2,4)$ using k-map.

(b) Briefly explain, why NAND and NOR gates are known as universal gates?

7. Attempt any *one* part of the following: 10 x 1 = 10

(a) Draw the block diagram of Digital Multi Meter (DMM). Explain the function of each block.

(b) Draw the block diagram of CRO. Also explain the function of each block.