Printed Pages : 4 EEC201/ECE201

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3302 Roll No. | | | | | | | | | | |

B.Tech.

(SEMESTER-II) THEORY EXAMINATION, 2011-12

ELECTRONICS ENGINEERING

Time : 3 Hours] *[Total Marks : 100*

Note : Answer **all** the Sections.

Section – A

1. Attempt **all** parts of this question : $10 \times 2 = 20$

(a) Distinguish between avalanche and zener breakdown.

(b) For p type semiconductor dopants from 3rd group are typically employed. Can we use dopants from 2nd group ? Give reason.

(c) Determine I_E, α and β of common base transistor circuit given $I_C = 7$ mA, $I_B = 0.1$ mA.

(d) The thickness of base is typically smaller than emitter and base. Why ?

(e) What is the basic difference between JFET and MOSFET ?

(f) What do you mean by term slew rate in opamp ?

(g) Convert 120_{10} to equivalent hexadecimal.

(h) What do you mean by canonical form of a Boolean expression ?

(i) How is voltage measured using CRO ?

(j) Describe input characteristics of a digital voltmeter.

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Section – B

2. Attempt any **three** parts of this question : **3 × 10 = 30**

(a) (i) Explain the formation of potential barrier across a p-n junction.

(ii) Explain the function of the circuit of Fig. 1 and draw the output waveform.

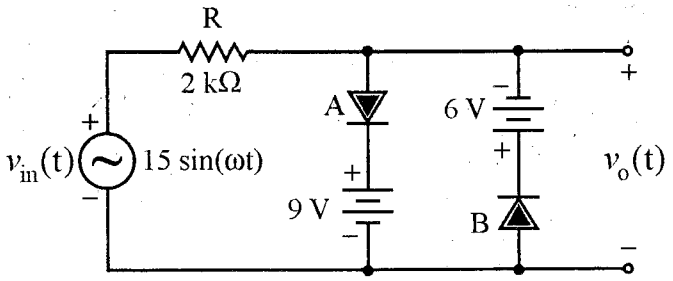

Fig. 1

(b) (i) What is base width modulation ? How it affects the output characteristics of a transistor in CB and CE configuration ?

(ii) The transistor in Fig. 2 has values of h_{FE} = 100. Determine the Q-point values of I_C and V_{CE} at both of these temperatures.

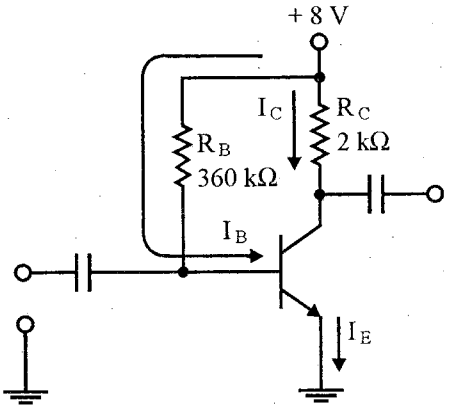

Fig. 2

(c) (i) Describe different biasing schemes used in JFET amplifiers. State their advantages.

(ii) Given I_{DSS} = 9 mA and V_P = –3.5 V, determine I_D when V_{GS} = 0 V and V_{GS} = –2V.

(d) (i) Represent the unsigned numbers 84 and 56 in BCD and then show the steps necessary to form their sum.

(ii) Express $(10110.0101)_2$ in decimal.

(e) (i) Explain how would you measure phase of signal from CRO.

(ii) Describe the operating of CRO with neat block diagram.

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Section – C

Attempt any **two** parts of each question : **5 × 10 = 50**

3. (a) Determine V_0 for the network for the input indicated.

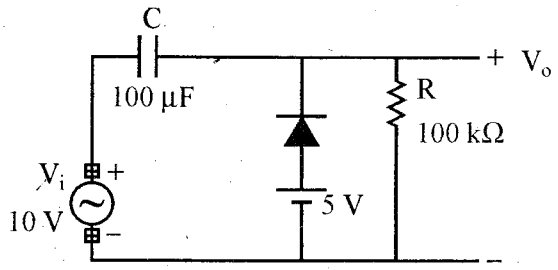

Fig. 3

(b) Explain the working of centre tap full wave rectifier. What is the value of peak inverse voltage ?

(c) Discuss the application of zener diode as shunt regulator.

4. (a) Draw hybrid equivalent of CE configuration and obtain expressions for A_I and A_V.

(b) Why is transistor biasing required ? Describe different schemes of transistor biasing in CE n-p-n transistor circuit. State their advantages.

(c) Determine R_i and R_o for the circuit of Fig. 4. Use the following parameters :

$h_{fe} = 110$, $h_{ie} = 1.6\ k\Omega$, $h_{re} = 0.0002$ and $h_{oe} = 20\ \mu A/V$, $R_C = 4.7\ k\Omega$, $R_B = 470\ k\Omega$.

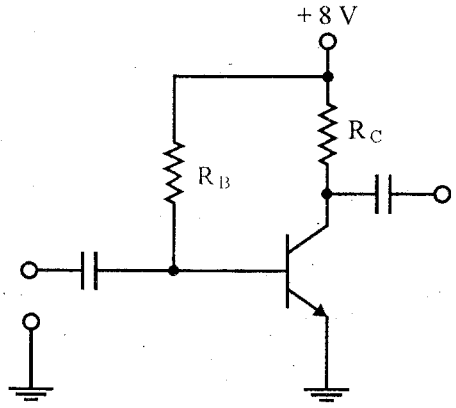

Fig. 4

5. (a) Explain the construction of depletion type NMOSFET and explain its output characteristics.

(b) Draw the circuit diagram of an integrator using opamp and explain its working.

(c) Describe ideal and practical opamp parameters.

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6. (a) Implement an OR gate using NAND gates.

(b) Simplify the following function with help of K map :

$$F(A, B, C, D) = \sum(3, 5, 9, 11, 15) + d\,(2, 4, 6, 10)$$

(c) Discuss the commutative and distributive postulates of Boolean algebra with example.

7. (a) Draw block diagram of digital multimeter and explain its working.

(b) Discuss different controls of CRO.

(c) What is function of time base circuit in CRO ? How will you measure the frequency of sinusoidal signal with help of CRO ?
