(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3034 Roll No. | | | | | | | | | | |

B.Tech.

SECOND SEMESTER EXAMINATION, 2005-2006

ELECTRONIC ENGINEERING

Time : 3 Hours *Total Marks : 100*

Note : *(i) Attempt ALL questions.*
(ii) All questions carry equal marks.
(iii) In case of numerical problems assume data wherever not provided.
(iv) Be precise in your answer.

1. Attempt ***any four*** parts of the following : **(5x4=20)**

(a) Distinguish between intrinsic and extrinsic semiconductors. What properties of a semiconductor are determined from Hall effect experiment ? Explain briefly.

(b) Describe the condition established by forward and reverse bias condition on a p-n junction diode and how the resulting current is affected ?

(c) What is static and dynamic resistance in the forward biasing of the diode ? Explain with suitable diagram.

(d) Draw a circuit diagram which uses a breakdown diode to regulate the output voltage across a load and explain the working.

(e) How does the diffusion capacitance C_D vary with dc diode current ? Explain.

(f) What do you mean by Zener and a Avalanche breakdown in the barrier layer of a semiconductor ?

2. Attempt ***any four*** parts of the following : **(5x4=20)**

(a) Explain the following terms in context with a semiconductor diode.

(i) Potential Barrier

(ii) Depletion layer

(iii) Breakdown voltage

(iv) Peak inverse voltage

(v) Knee voltage

(b) For the given zener diode network shown in figure 2 (b) determine V_L, V_R, I_Z, and I_R.

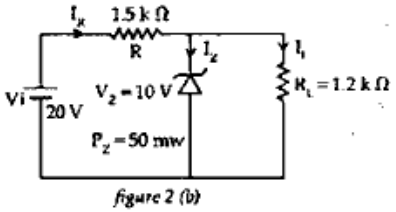


figure 2 (b)

(c) A 220V, 50 Hz ac. voltage is applied to the primary of 4 : 1 step-down transformer, which is used in a bridge rectifier, having a load resistance of 1 $k\Omega$. Assuming the diodes to be an ideal, determine the following :

(i) D.C. output voltage

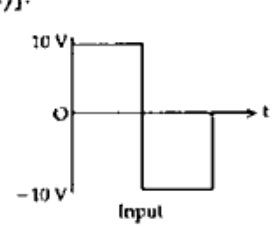
(ii) DC. Power delivered to load

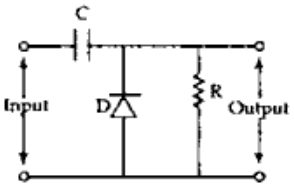
(iii) PIV of each diode

(iv) Output frequency

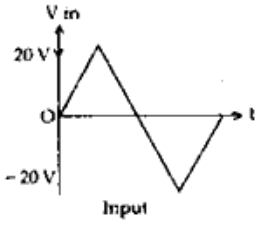
(d) Draw the output waveform for the following circuit for the given input waveform [Ref to figure 2 (d)].

(i)





(ii)



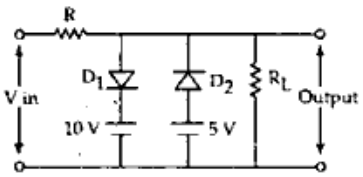


figure 2 (d)

(e) Draw the voltage double circuit and the working of the circuit.

(f) Draw a neat diagram of a full wave bridgerl rectifier circuit. Explain its working in details, clearly making the direction of flow of currents for positive and negative cycles.

3. Attempt ***any four*** parts of the following : **(5x4=20)**

(a) For the given network shown in figure 3 (a) determine the I_C, V_{CE}, V_B and V_C.

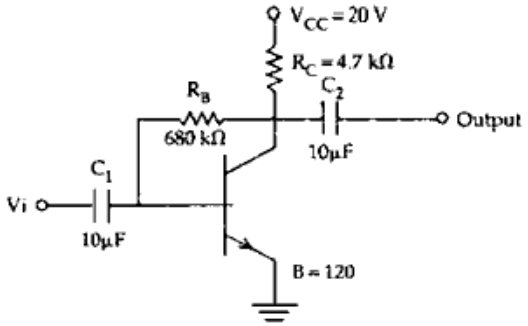


figure 3 (a)

(b) Draw the circuit diagram of transistor in the CE configuration. Sketch the output characteristics and indicate the active, saturation and cut off region.

(c) A junction transistor has the following h-parameters $h_{ie} = 2k$ $h_{re} = 1.6 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 50$ $\mu A/V$ Determine the current gain, voltage gain, input resistance and output resistance of CE amplifier if the load resistance is 12 kΩ and source resistance is 500 Ω.

(d) Draw the hybrid equivalent circuit for common basic configuration and find the expression of current gain, voltage gain and input impedance.

(e) Draw the d.c. load line and locate the operating point for the fixed biasing transistor circuit shown in figure 3 (e). What will be its stability factor. $V_{BE} = 0.7V$.

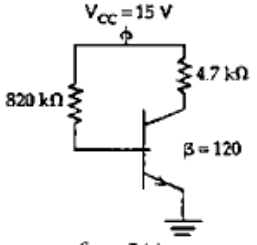


figure 3 (e)

(f) Why a capacitive coupling is used to connect a signal source to an amplifier ? For a capacitively coupled load, is the dc load larger or smaller than ac load ? Explain.

4. Attempt ***any two*** parts of the following : **(10x2=20)**

(a) What is the significant difference between the construction of an enhancement type MOSFET and depletion type MOSFET ? Explain with suitable diagram.

(b) Determine the following for the given network shown in figure 4(b).
I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS}, V_{DG}

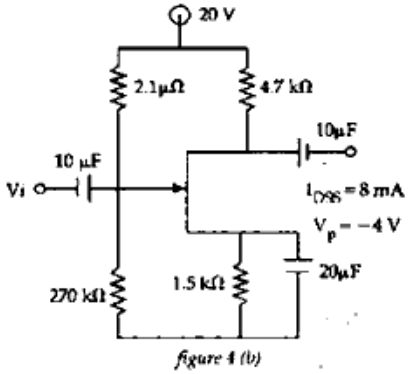


figure 4 (b)

(c) What are the advantages of the FET over a conventional bipolar junction transistor ? Define pintch-off voltage, amplification factor and drain resistance of FET. Explain with the help of circuit diagram, how an FET is used as a voltage dependent resistor.

5. Attempt *any two* parts of the following : **(10x2=20)**

(a) (i) Convert the following function in to canonical form

(1) $AB + B\overline{C}D + \overline{A}D$

(2) $(A + \overline{B})(\overline{C} + \overline{D})(\overline{B} + \overline{C})$

(ii) Convert the following numbers

(1) $(4021.25)_{10} = (\quad)_2$

(2) $(A6F.CD)_{16} = (\quad)_8$

(iii) Solve the following :

(1) $(A6C.DF)_{16} + (IDE.9A)_{16}$

(2) $(7001)_8 - (5763)_8$

(iv) Minimize the give boolean function with the help of Boolean Algebra rules

$$f(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BCD + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}\,\overline{C}D + A\overline{B}C\overline{D} + AB\overline{C}\,\overline{D} + AB\overline{C}D + ABC\overline{D}$$

(b) (i) Minimize the given Boolean function using k-map

f (A, B, C, D) $= \Sigma$ m (3, 4, 5, 7, 9, 13, 14, 15) + d (0, 2, 8)

Implement the minimized function only using NAND gates.

(ii) Prove that the NAND and NOR gate is a universal gate.

(c) (i) Explain the terms in op-Amp.

(1) Input off set current

(2) Input off set voltage

(3) Slew Rate

(4) CMRR

(ii) Draw the circuit diagram of op-Amp as summer and subtractor and find out the expression for output.

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