Printed Pages : 7 **TEC – 101 / TEC-201**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3033/3034 Roll No.

B. Tech. (Sem. I & II)

SPECIAL CARRYOVER EXAMINATION, 2006-07

ELECTRONICS ENGINEERING

Time : 3 Hours] *[Total Marks : 100*

Notes : *(1) Attempt **all** questions.*

(2) Number of parts to be attempted from each question are indicated.

1 Answer any **four** parts from the following : **4×5**

(a) Comment on any **two** from the following statement :

(i) Electron and hole recombine and disappear.

(ii) An intrinsic semiconductor have equal number of electrons and holes.

(iii) A semiconductor behaves like an insulator at 0^{o}k and becomes conductor at room temperature.

(b) Draw the V-I characteristic of p-u junction diode. Write the current-voltage equation, specify all terms of equation. Discuss its temperature dependance.

(c) Discuss the capacitive effect of p-u junction under reverse bias. What will happen to capacitance if the polarity of the applied voltage is changed explain ?

(d) At what voltage the reverse current flowing through a germanium diode will reach 90% of it's saturation value at room temperature 27°C ?

(e) Define static and dynamic resistance of diode. How it can be obtained ?

(f) Calculate V_0 and I_D for the circuit given in **fig. 1**.

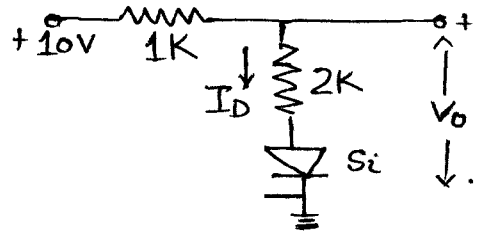

Fig. 1

2 Attempt any **two** parts from the following : **2×10**

(a) (i) Draw the circuit diagram of a full wave rectifier with π filter whose PIV = Vm.

(ii) Define voltage regulation. Derive the expression for regulation and show that it is same in Half wave rectifier and full wave rectifier.

(b) (i) What is the difference between avalanche breakdown and zener breakdown of a p-u junction ? Draw the circuit diagram of voltage regulator using zener diode.

(ii) Calculate the V_{DC}, I_{DC}, $V_{r(rms)}$, I_{rms} through 1 kohm load connected to half wave rectifier circuit shown in **fig. 2**.

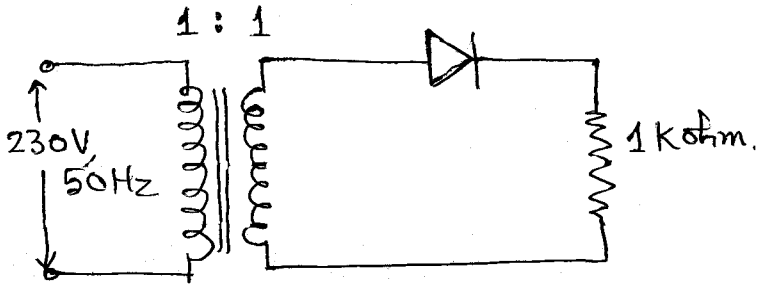

Fig. 2

(c) (i) Prove that maximum d.c. output power occurs in half wave rectifier when $R_f = R_L$.

(ii) Write short notes on any **two** of the following :

(i) Voltage multiplier circuit using diodes.

(ii) Clipping circuits

(iii) Different type of filters used in rectifiers.

3 Attempt any **two** parts from the following : **2×10**

(a) (i) Draw the output characteristic curve of n-p-n transistor in CE configuration level the parameters and indicate different regions of operation.

(ii) A germanium transistor used in an amplifier has a collector cut off current $I_{CO} = 10\ \mu A$ at a temperature of 20°C and $h_{FE} = 50$, find collector current when.

(i) The Base current is 0.25 mA.

(ii) Assuming h_{FE} does not increase with temperature and temperature rises to 50°C.

(b) (i) What do you understand by "Transistor biasing" ? Mention the important points to be considered for the selection of operating point.

(ii) A Germanium transistor with β-49 has the potential divider arrangement with $R_L = 1$ kohm, $V_{CE} = 5$ V, $I_C = 4.9$ mA and $V_{BE} = 0.2$ V. The stability factor is desired to be 10. Obtain the values of biasing resistors R_1, R_2 and R_E. Draw the circuit diagram also.

(c) Draw the low frequency hybrid model of transistor amplifier in CE configuration given in **fig. 3** (c) and calculate input resistance, current gain and voltage gain of the amplifier. Given $h_{ie} = 1$ k, $h_{re} = 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 100\ \mu$ mho.

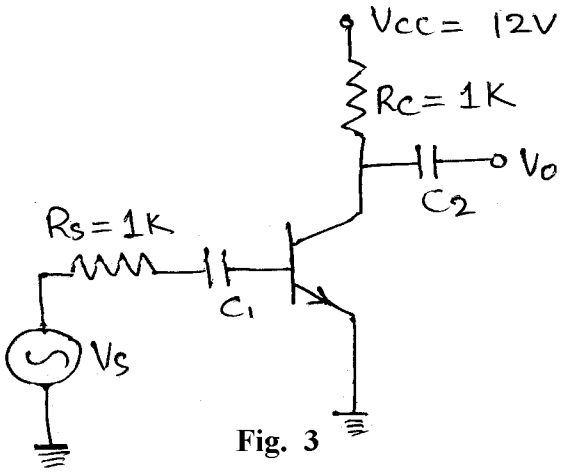

Fig. 3

4 Answer any **four** parts from the following : **4×5**

(a) Explain the phenomenon of "Pinch off" in JFET.

An n channel silicon JFET has a donor concentration of $2 \times 10^{21}/m^3$ and a channel width of 4 μm. If the dielectric constant of S_i is 12, find the pinch off voltage.

(b) Why FET is called voltage controlled device ? Draw the circuit diagram of JFET common drain amplifier and derive the expression for its voltage gain.

(c) In a self bias n channel JFET, the operating point is to be set at $I_D = 1.5$ mA and $V_{DS} = 10$ V. The JFET parameters are $I_{DSS} = 5$ mA and $V_P = -2V$. Find the value of R_S and R_D for given $V_{DD} = 20$ V, draw the circuit diagram also.

(d) Write the basic difference between enhancement and depletion MOSFET. Draw the structure of P-channel depletion MOSFET and explain working with drain and transfer characteristics.

(e) Draw the structure of n channel JFET its drain and transfer characteristics. Indicate the different regions of operation in the drain characteristics. Why the name is "Field Effect Transistor" ?

(f) Discuss different biasing methods of JFET.

5 Attempt any **four** parts from the following : **4×5**

(a) Convert the following as directed :

(i) $(62.7)_8 = (-----)_{16}$

(ii) $(0.342)_6 = (-----)_{10}$

(iii) $(10.10001)_2 = (-----)_8$

(iv) $(1\ BE)_{16} = (-----)_8$

(v) $(547)_{10} = (BCD\ code)$

(b) Simplify one of the following Boolean expressions and implement the result as a logic diagram :

(i) $AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$

(ii) $AB + A\bar{B}C\left(\overline{BC} + C\right) + \overline{AC}$

(c) Reduce the following using K Map.

$$f(A, B, C, D) = \sum M\,(0, 1, 2, 11, 12, 14, 15) + d\,(3, 5, 6, 13)$$

(d) Draw the pin diagram of 741 Op-Amp and mention the function of each pin. What are the characteristics of an ideal Op-Amp ? Why it is called operational amplifier ?

(e) Calculate the maximum and minimum closed loop gain for the amplifier shown in **fig. 4** (e) assuming ideal Op-Amp.

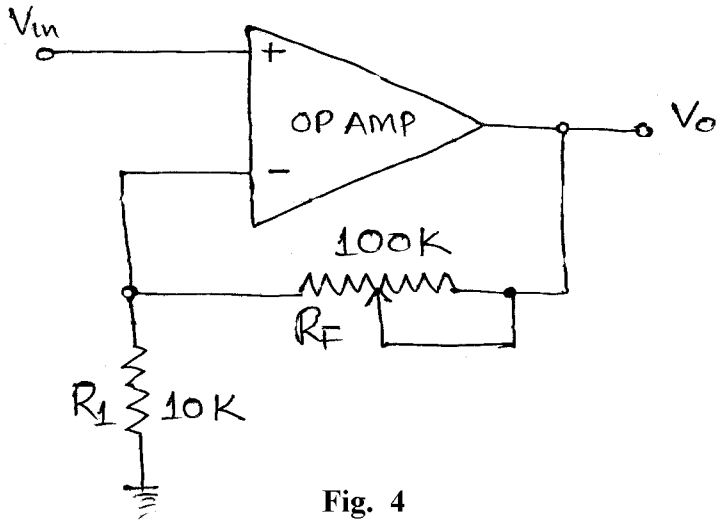

Fig. 4

(f) State and prove DeMorgan's theorem.
