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TEC—101

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3033 Roll No. | | | | | | | | | | |

B.Tech.

FIRST SEMESTER EXAMINATION, 2005-2006

ELECTRONICS ENGINEERING

Time : 3 Hours *Total Marks : 100*

Note : *(i) Answer **ALL** questions.*

(ii) All questions carry equal marks.

(iii) In case of numerical problems assume data wherever not provided.

(iv) Be precise in your answer.

1. Attempt ***any four*** of the following questions : **(5x4=20)**

(a) Distinguish between intrinsic and extrinsic semiconductor. What is the effect of temperature on conductivity of a semiconductor ?

(b) How are the carrier mobilities related with resistivity of a semiconductor ? Does a 'hole' in a semiconductor contribute to a flow of current ? If yes, how and if no, how ?

(c) Discuss the current flow mechanism in a p-n junction under -

(i) no bias

(ii) forward bias

(iii) reverse bias conditions.

(d) A germanium diode carries a current of 1mA at room temperature when a forward bias of 0.15V is applied. Estimate the reverse saturation current at room temperature.

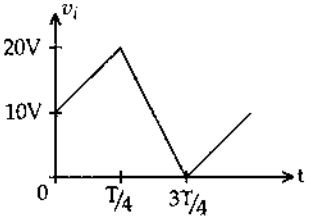
(e) Which is more sensitive to a change in temperature, forward current or reverse current ? Explain why ?

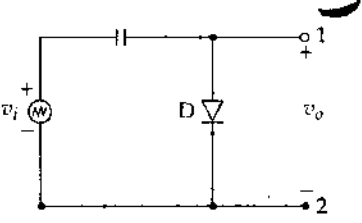
(f) Explain, the transition capacitance and diffusion capacitance of a p-n junction.

2. Attempt *any two* of the following questions : **(10x2=20)**

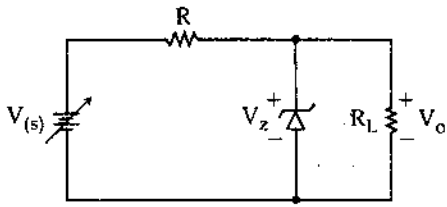
(a) What is transformer utilisation factor ? Determine the rating of a transformer to deliver a 100 Watts of d.c. power to a load under full wave rectifier.

(b) Distinguish between clipping and clamping circuits. Draw the waveform observed on an oscilloscope in dc mode when connected between 1 and 2 of the following circuit with shown v_i applied. Indicate voltages and the zero level. Also give the numerical values of the reading of a d.c. voltmeter connected across 1 and 2. Find the PIV of the diode.





(c) Explain 'Avalanche' break down. Draw the *v-i* characteristics of zener diode and explain how does a zener regulate a voltage ? The input voltage for the following figure varies from 35V to 45V, $V_Z = 20V$ $r_Z = 5\Omega$ $I_L(min) = 0mA$, $I_L(max) = 100mA$, $Iz(min) = 10mA$, $Iz(max) = 400mA$. Find the values of R and P_Z (max).



3. Attempt *any four* of the following questions : **(5x4=20)**

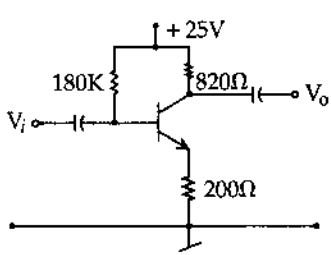
(a) Define with respect to BJT the following.

(i) I_{CO} (ii) α (iii) β

(iv) I_{CEO} (v) I_{CBO}

(b) Draw and explain the input and output charecteristics of common base configuration of BJT. Indicate all the region of operations.

(c) Find Ic and V_{CE} for the following circuit if $\beta = 80$ for the BJT.



(d) The collector and base current of n-pn transistor are measured as $I_c = 5$ mA, $I_B = 50\mu A$ and $I_{cBo} = 1\mu A$.

(i) Determine α, β and I_E.

(ii) Determine the new level of I_B required to produce $I_c = 10$ mA.

(e) Explain how operating point is selected for amplification in CE mode using Graphical method only.

(f) Derive the voltage gain, current gain expressions for a potential devider biased common emitter amplifie using h parameters.

4. Attempt *any two* of the following questions : **(10x2=20)**

(a) Write notes on the following :

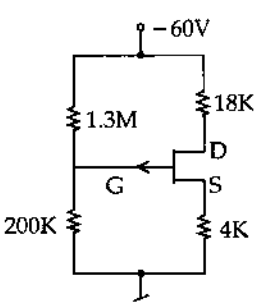
(i) depletion type MOSFET

(ii) Pinch-off voltage

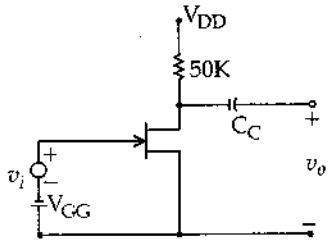
(iii) Transfer characteristics of JFET

(iv) Transconductance

(b) Consider the following circuit. Determine I_D, V_{GS} and V_{DS} for $|I_{DSS}| = 4$ mA, $Vp = 4V$.

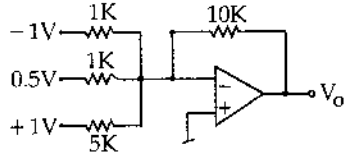


(c) Calculate the voltage gain and output resistance of the following circuit. Given that gm = 2mA/V and v_d = 10k.

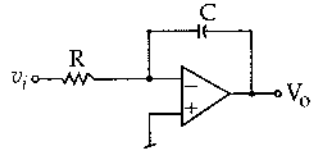


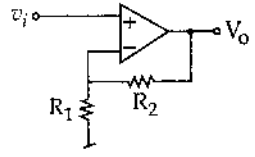
5. Attempt *any four* of the following questions : **(5x4=20)**

(a) Enlist the ideal characteristics of an op-amp. Why op-amp is called operational amplifier. Find out the voltage output of the following circuit.



(b) Determine the output of both of the circuits.





(c) Convert the following numbers as indicated :

(i) $(1001)_8 = (\quad)_2$

(ii) $(2CCD)_{16} = (\quad)_5$

(iii) $(0.45)_{10} = (\quad)_8$

(iv) $(345)_8 = (\quad)_{10}$

(v) $(7841)_9 = (\quad)_{10}$

(d) (i) Realise AND, OR, NOT using only NAND gates.

(ii) Using NOR gates only realise Ex – OR gate.

(e) Minimise using K-Map f (A, B, C, D) = Σ(1, 3, 5, 7, 9, 11, 13, 15) then convert the minimised function into POS.

(f) Write notes on the following :

(i) Demorgan's Theorem

(ii) Canonical form of Boolean function

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